REMARKS

Prior to the examination of the present application, claim 1 is canceled without prejudice or waiver, and claims 31-62 are added. Claims 2-30 were previously canceled in the transmittal of the application on September 19, 2003. Claims 31-62 remain in the application. It is not the Applicants' intent to surrender any equivalents because of the amendments or arguments made herein. Examination and consideration of the application, as amended, are respectfully requested.

It is submitted that this application is in good order for allowance and such allowance is respectfully solicited. If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6742 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: October 8, 2003

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Amendments to the Specification

Please amend the title of the invention as follows:

~~SEMICONDUCTOR DEVICE~~ NAND FLASH MEMORY

Please amend the BRIEF SUMMARY OF INVENTION on Page 9, line 5 through page 10, line 9 as follows:

~~A semiconductor device according to a first aspect of the present invention comprises first and second lines arranged with a first interval, and third and fourth lines arranged with a second interval wider than the first internal; wherein the first internal is a minimum interval less than 0.12 μm, and a maximum value of a voltage generated between the third and fourth lines is greater than a maximum value of a voltage generated the first and second lines.~~

~~A semiconductor device according to a second aspect of the present invention comprises first and second lines in a wiring layer arranged with a first interval, a third line arranged in the wiring layer, wherein a second interval between the first and third lines is wider than the first interval, and a first transistor configured to connect the second and third lines; wherein the first interval is a minimum interval less than 0.12 μm, and a maximum value of a voltage generated between the first and third lines is greater than a maximum value of a voltage generated between the first and second lines.~~

~~A semiconductor device according to a third aspect of the present invention comprises first and second lines in a wiring layer arranged with a first interval, a third line arranged in the wiring layer, and a first transistor configured to connect~~

~~the second and third lines; wherein the first interval is a minimum interval less than 0.12 μm, and a maximum value of a voltage generated between the first and third lines is greater than a maximum value of a voltage generated the first and second lines, and the third line is arranged at a position not adjacent to the first line.~~

A NAND flash memory according to an aspect of the present invention comprises a NAND memory cell array having a NAND block which comprises NAND memory cells; first and second lines arranged in the NAND block with a first interval, connected to the NAND memory cells; and third and fourth lines arranged in the NAND block with a second interval wider than the first interval; wherein the first interval is a minimum interval less than 0.12 μm, and a maximum value of a voltage generated between the third and fourth lines is greater than a maximum value of a voltage generated between the first and second lines.